where s_0 is the width of n-type region **2** across its cross section, D is the depth of n-type region **2**, l is the height of n-type region **2**, q is the amount of the elementary electric charge, ρ_{n0} is the n-type net doping concentration, and μ_n is the electron mobility.

[0010] In the case of the profile indicated by the broken line in FIG. **2**B in which mutual diffusion is taken into consideration, the electric conductance σ_2 of the n-type region **2** is given by

$$\sigma_2=\int q\rho_n(s)\mu_n D ds/l(\Omega^{-1}) \quad (2)$$

where $\rho_n(s)$ is the net doping concentration distribution along the cutting line, and s is the position on the cutting line. The integration is done over the width of the n-type region **2**. If the mobility is constant, Equation (2) is modified as follows:

$$\tau_2=q\mu_n D\int\rho_n(s)ds/l \quad (3)$$

[0011] Since the total net doping of n-type region **2** in the case with mutual diffusion is equivalent to that of the case without mutual diffusion, a relationship

$$Dl\int\rho_n(s)ds=s_0 Dl\rho_{n0} \quad (4)$$

holds. From equations (3) and (4), we obtain

$$\sigma_2=q\mu_n Ds_0\rho_{n0}/l=\sigma_1. \quad (5)$$

[0012] That is, the on-resistance in the case with mutual diffusion is equal to that in the case without mutual diffusion. However, in actuality, although the total net doping is the same, the total doping concentration (i.e., the sum of the p-type doping concentration and the n-type doping concentration) increases due to the mutual diffusion and hence the mobility decreases a little (the mobility depends on the total doping concentration). Therefore, the resistance of n-type region **2** is a little increased by the mutual diffusion.

[0013] As described above, even if mutual impurity diffusion occurs between p-type regions (columns) **3** and n-type regions (columns) **2** because the SJ column structure is subjected to thermal history, the on-resistance/breakdown voltage tradeoff is hardly deteriorated. However, this is true only under ideal conditions that the concentrations of introduced impurities have no variations.

[0014] In practice, the p-type and n-type impurity concentrations vary due to variations in a manufacturing process. For example, assume a junction, having a step-like profile, of a p-type region (column) and an n-type region (column) each of which has an impurity concentration of 1×10^{15} cm^{-3}. If it is assumed that the variation of each impurity concentration due to variations in a manufacturing process is $\pm10\%$, that is, $\pm1\times10^{14}$ cm^{-3}, in the worst case the p-type concentration becomes 1.1×10^{15} cm^{-3} and the n-type concentration becomes 0.9×10^{15} cm^{-3}; the charge balance between the p-type region and the n-type region is calculated as 1.1/0.9=122%. This charge imbalance lowers the breakdown voltage.

[0015] Next, consideration will be given to the case in which there is mutual diffusion. For example, assume that the doping concentration of each of the p-type region (column) and the n-type region (column) is decreased by 1×10^{15} cm^{-3} by the mutual diffusion (since the doping effects of the pair of dopants, that is, the p-type dopant and the n-type dopant, cancel each other out, the decrease in the doping concentration of the p-type region (column) is equal to that in the doping concentration of the n-type region (column)). It is necessary that the concentration of each of the p-type region (column) and the n-type region (column) before the SJ column structure be subjected to thermal history be set at 2×10^{15} cm^{-3} (step-like profile). If it is assumed that the variation of each impurity concentration due to variations in a manufacturing process is $\pm10\%$, that is, $\pm2\times10^{14}$ cm^{-3}, and that the doping concentration is decreased by 1×10^{15} cm^{-3} by the mutual diffusion, in the worst case the concentration of the p-type region (column) becomes 1.2×10^{15} cm^{-3} and the concentration of the n-type region (column) becomes 0.8×10^{15} cm^{-3}; the charge balance between the p-type region (column) and the n-type region (column) is calculated as 1.2/0.8=150%. This charge imbalance lowers the breakdown voltage to a large extent. As is understood from the above discussion, in the case with mutual diffusion, the influence of variations in a manufacturing process is amplified when it is intended to obtain the same electrical characteristics. The breakdown-voltage-related yield is thereby lowered.

[0016] In the manufacturing method of the buried-trench SJ-MOSFET, the factors causing variations in the impurity concentrations of the p-type regions (columns) and the n-type regions (columns) include variations of the impurity concentration of the n-type epitaxial regions, the impurity concentration of the p-type buried epitaxial regions, the trench width, and the trench taper angle. These factors cause a charge imbalance between the p-type regions (columns) and the n-type regions (columns). If the thermal history is made more severe, the influence of the above variations becomes more serious. One method for preventing the breakdown-voltage-related yield from being lowered even if the thermal history is made more severe is to set the original impurity concentrations of the p-type regions (columns) and the n-type regions (columns) low. However, these impurity concentrations cannot be set low because doing so increases the on-resistance. Therefore, it can be said that it is desirable to decrease the number of thermal history events that cause mutual diffusion after formation of the p-type regions (columns) and n-type regions (columns).

[0017] In connection with the manufacturing method of the above-described buried-trench SJ-MOSFET, US-A1-2003-0008483 (corresponding to JP-A-2002-83962) is known which discloses a manufacturing method of an SJ-MOSFET which employs a super-junction structure in which a drift region is a collection of column-shaped p-type and n-type regions that are arranged in parallel and in close contact with each other on a low-resistivity semiconductor substrate and extend perpendicularly to its major surface. Furthermore, in this manufacturing method, deterioration of the characteristics is prevented by decreasing the number of thermal history events to which the super-junction structure is subjected in post manufacturing steps.

[0018] However, according to the disclosure of US-A1-2003-0008483, in the manufacturing method of an SJ-MOSFET, in the case where the breakdown voltage rating is 600 V, the thickness (in the direction perpendicular to the major surface of the substrate) of the SJ column structure that is necessary for attaining such a breakdown voltage is about 50 μm. An SJ-MOSFET is manufactured by forming MOS gate structures on the front side, decreasing the wafer thickness to about 50 μm by grinding the back surface, and